

# **EXHIBIT**

# **E**

# SMP402

## 1-Watt Buck Regulator IC

### 20-72 VDC Input

### Non-isolated DC Output



#### Product Highlights

##### Integrated Power Switch and CMOS Controller

- Output power > 1 W from 48 VDC input
- Adjustable output voltage
- Integrated solution minimizes overall size

##### High-voltage, Low-capacitance MOSFET Output

- Designed for ISDN T1 telecommunications applications
- Low capacitance allows for high frequency operation

##### High-voltage Buck Regulator

- Internal pre-regulator self-powers the IC on start-up
- Designed for low power consumption
- Minimum external parts required

##### Built-In Self-protection Circuits

- Undervoltage lockout
- Thermal shutdown
- Input polarity/level sense

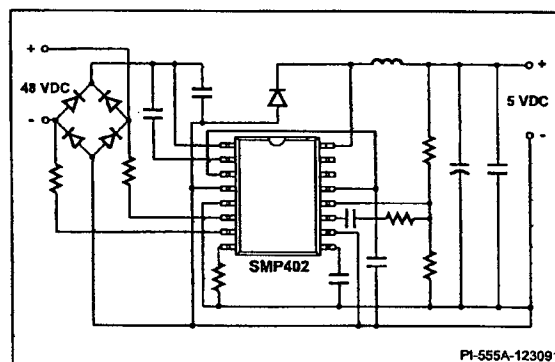


Figure 1. Typical Application.

## Description

The SMP402, intended for non-isolated ISDN telecommunications power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost power supply which meets stringent ISDN specifications. High frequency operation reduces total power supply size.

The P-channel power MOSFET switch features include high voltage, low  $R_{DS(ON)}$ , and low capacitance. Lower capacitance results in a reduction in gate drive power, and also facilitates higher frequency operation.

The controller section of the SMP402 contains all the blocks required to drive and control the power stage: start-up pre-regulator circuit, oscillator, bandgap reference, error amplifier, gate driver and level shift. Protection features include undervoltage lockout, thermal shutdown, and input polarity and level sensing.

The SMP402 is available in a 16-pin plastic SOIC package.

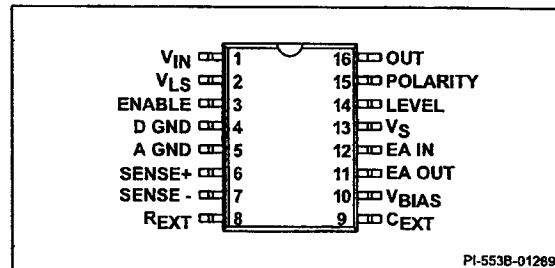


Figure 2. Pin Configuration.

ORDERING INFORMATION		
PART NUMBER	PACKAGE OUTLINE	T <sub>J</sub> RANGE
SMP402SC	S16A	0 to 120°C

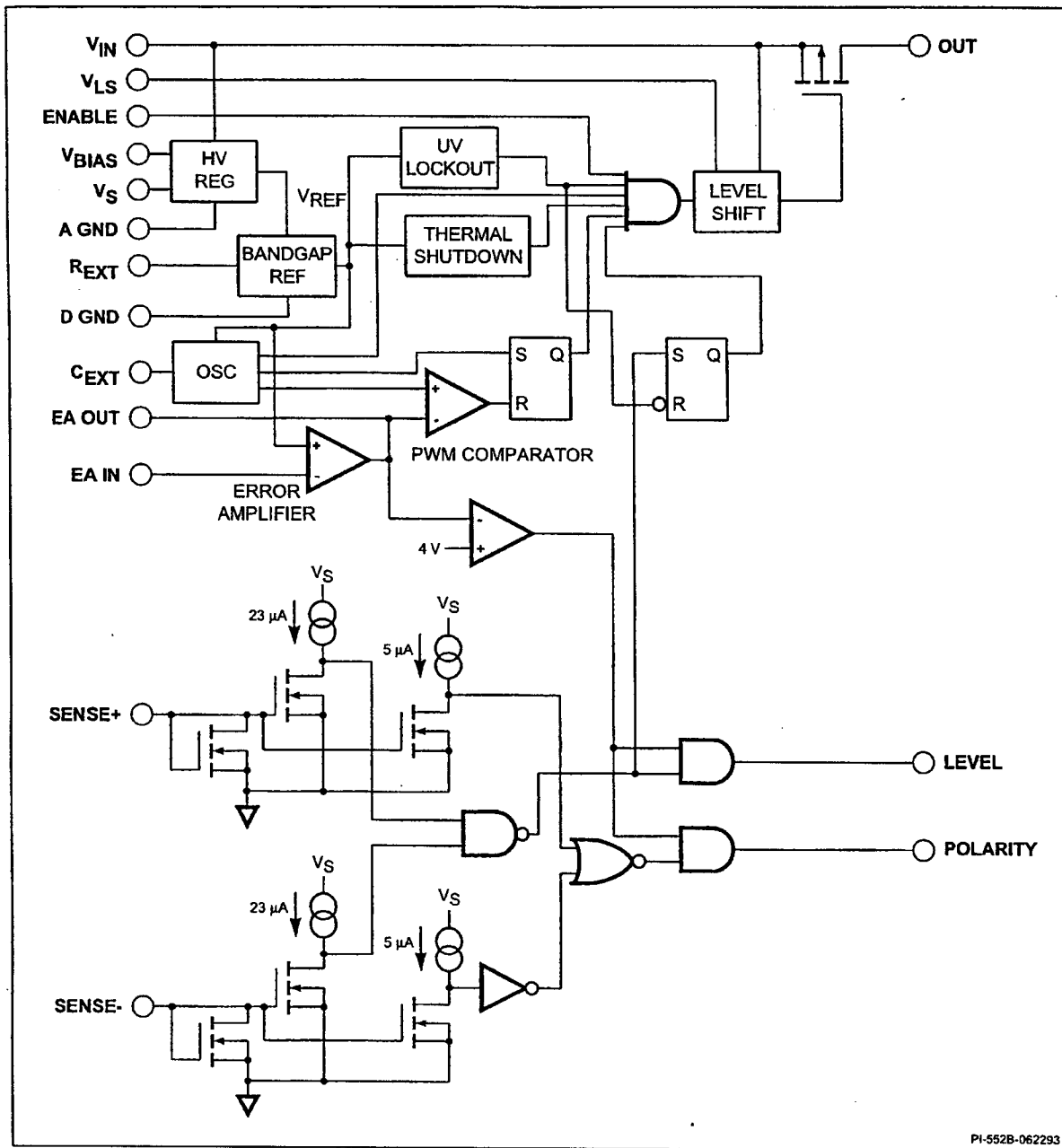
**SMP402**

Figure 3. Functional Block Diagram.

## Pin Functional Description

### Pin 1:

$V_{IN}$  is the high-voltage input to the switching regulator. This is the Source connection of the P-Channel power MOSFET pass transistor.

### Pin 2:

$V_{LS}$  is an internal supply for the level shift circuit that drives the P-Channel MOSFET. A capacitor should be placed between  $V_{LS}$  and  $V_{IN}$  for bypassing.  $V_{LS}$  is normally 10 V below  $V_{IN}$ .

### Pin 3:

The power supply can be shut down by pulling **ENABLE** low.

### Pin 4:

**D GND** is the common return point for the power and logic portions of the circuit.

### Pin 5:

**A GND** is the common return point.  $R_{EXT}$  and  $C_{EXT}$  are directly connected to this point.

### Pin 6:

The **SENSE+** input monitors the polarity and level of the input voltage through an external resistor for ISDN emergency standby sensing.

### Pin 7:

The **SENSE-** input monitors the polarity and level of the input voltage through an external resistor for ISDN emergency standby sensing.

### Pin 8:

A 20.5 k $\Omega$  resistor connected between  $R_{EXT}$  and **A GND** sets the internal bias currents including oscillator charge and discharge currents.

### Pin 9:

The oscillator frequency can be programmed by selecting the value of the capacitor connected between  $C_{EXT}$  and **A GND**.

### Pin 10:

$V_{BIAS}$  can be connected to the output 5 V rail of the converter to reduce power dissipation. The internal 5 V regulator is cut off when the output is in regulation.

### Pin 11:

**EA OUT** is the error amplifier output pin for connection to the external compensation network.

### Pin 12:

**EA IN** is the error amplifier negative input for connection to the feedback and compensation networks.

### Pin 13:

$V_S$  is the internal supply voltage. This pin is brought out for external bypassing.

### Pin 14:

The **LEVEL** output indicates when the input voltage is in its normal operating range.

### Pin 15:

The **POLARITY** output is used to notify a microprocessor of an emergency standby condition for ISDN applications.

### Pin 16:

**OUT** is the Drain connection of the P-Channel pass transistor.

## Functional Description

### High Voltage Regulator

The high-voltage regulator provides the bias current required by the controller and driver circuitry. The pre-regulator consists of a high voltage MOSFET, a gate bias current source, and an error amplifier. The error amplifier regulates  $V_S$  to approximately 5 V by controlling the gate of the MOSFET.

In 5 V output applications, the control circuitry may also be operated by connecting the  $V_{BIAS}$  pin to the output 5 V rail of the converter to reduce power dissipation. The internal 5 V regulator is cut off automatically when the converter output is in regulation. Only the supply

current for the level shift stage ( $\approx 50 \mu A$ ) and the AC switching currents for the P-Channel output device are drawn from the  $V_{IN}$  supply under this condition. If unused,  $V_{BIAS}$  must be hardwired to **A GND** to disable the automatic switchover during power-up.

$V_{LS}$  is the level-shift supply for driving the gate of the internal P-channel MOSFET. The voltage at  $V_{LS}$  is approximately 10 V below  $V_{IN}$ .  $V_S$  is the supply voltage for the controller and driver circuitry. External bypass capacitors connected to  $V_{LS}$  and  $V_S$  are required for filtering and reducing noise.

### UV Lockout

During power-up, the undervoltage lockout circuit keeps the P-channel output transistor in the off state until the internal  $V_S$  supply is in regulation and the voltage sensed by the input monitor circuit is within the normal operation range ( $>12 V$ ).

### Band Gap Reference

$V_{REF}$  is the 1.3 V reference voltage generated by the temperature-compensated bandgap reference and buffer. This voltage is used for setting thresholds for the error amplifier and over temperature circuit.



**SMP402****Functional Description (cont.)****Oscillator**

The oscillator frequency can be adjusted by changing the external  $C_{EXT}$  capacitor. This capacitor is charged and discharged by switched constant current sources.

The voltage switch points are determined by hysteresis built into a comparator. The period of the waveform is determined by values of the current sources which set the rising and falling slopes of the sawtooth waveform. Maximum duty cycle is equal to the ratio of the charge time to the period. Clock and blanking signals are synthesized from the comparator output for use by the modulator.

**Error Amplifier**

The error amplifier consists of a high performance operational amplifier with the non-inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the power switch.

**Pulse Width Modulator**

The pulse width modulator implements a voltage-mode control loop, and generates the digital driver signal which controls the power switch. The duty cycle of the driver signal will change as a function of input voltage and load. Increasing the duty cycle causes the power supply output voltage to go up. Conversely, decreasing the duty cycle causes the output voltage to go down. The pulse width modulator compares the control voltage (error amplifier output) with the sawtooth voltage generated by the oscillator to produce the required duty cycle.

**Thermal Shutdown**

Temperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 140°C). The device will automatically reset and turn back on again when the junction has cooled past the hysteresis temperature level.

**SENSE+ and SENSE- Inputs**

SENSE+ and SENSE- are both current mirror inputs consisting of N-channel MOSFETs connected as diodes. The threshold voltage of each transistor is typically 1.7 V. An input current which exceeds the indicated threshold current will turn on the mirror transistor for an active-low signal.

**POLARITY and LEVEL Outputs**

The LEVEL output is high when the input current to either SENSE+ or SENSE- exceeds the LEVEL current threshold and the output voltage is in regulation. During normal operation, the POLARITY output is high when the input current to SENSE+ is above the POLARITY current threshold and the output voltage is in regulation. During emergency operation (when the DC input voltage is inverted), the POLARITY output is low when the input current to SENSE- exceeds the

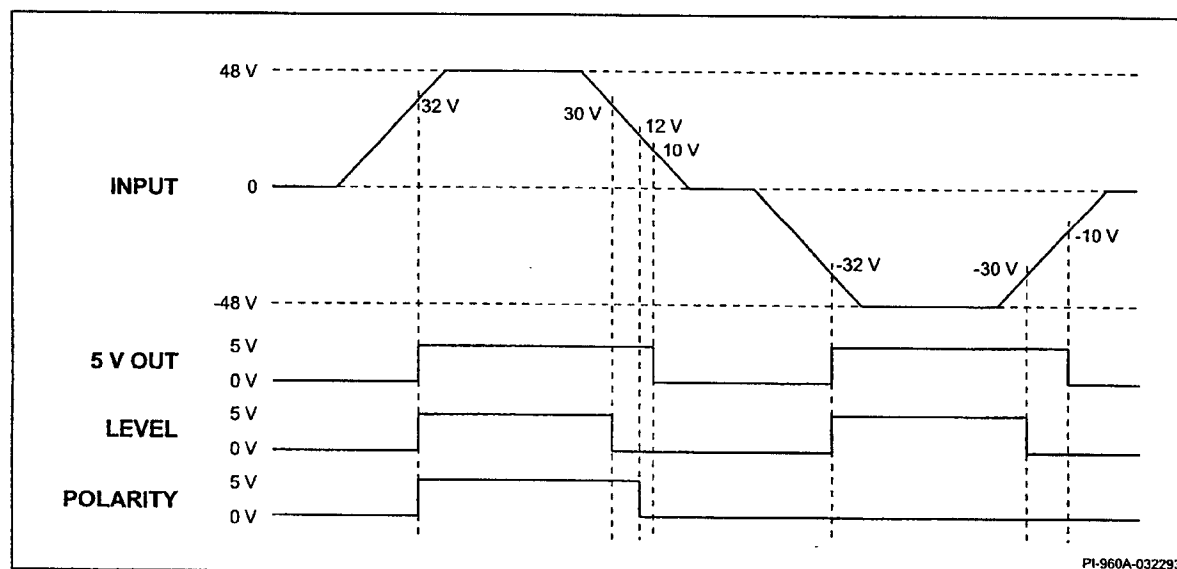


Figure 4. Turn-on and Turn-off Waveforms of the SMP402.



## Functional Description (cont.)

**POLARITY** current threshold. Regulation of the output voltage is detected by a comparator which looks for error amplifier saturation in the output high (maximum duty cycle) state.

Power supply turn on and turn off with a slowly changing input voltage is shown in Figure 4 as measured using the circuit shown in Figure 6. Also shown are the level and polarity outputs. The input voltage must rise above 32 V before the SMP402 will turn on. At this input voltage the current through R1 into the SENSE+ input exceeds the threshold current (typically 23  $\mu$ A), the LEVEL and POLARITY outputs go high, and

the power supply turns on. As the input voltage goes down, LEVEL will go low at approximately 30 V, but POLARITY will stay high. As the input voltage continues to drop, POLARITY goes low at approximately 12 V and the converter loses regulation at approximately 10 V and turns off. The LEVEL output will go high and the power supply turns on when the input voltage reaches -32 V. POLARITY stays low to indicate that the input voltage has reversed polarity. As the negative input voltage falls toward zero, LEVEL goes low at approximately -30 V and the converter loses regulation and turns off at approximately -10 V.

### Enable

The power supply can be shut down by pulling the ENABLE pin low. It is internally pulled up to  $V_s$  with a 100  $\mu$ A (nominal) current source. However, it is recommended that this pin be tied to  $V_s$  if it is unused.

### P-Channel Output Transistor

The output MOSFET is a 90 V pass transistor capable of supplying >200 mA. To minimize switching noise and EMI, it is important to keep the path from OUT through the output diode, the input storage capacitor, and into  $V_{IN}$  as short as possible.

INPUT VOLTAGE CONDITION	POLARITY	LEVEL
Negative voltage, level too low	0	0
Negative voltage, correct level	0	1
Positive voltage, level too low	1	0
Positive voltage, correct level	1	1

Figure 5. LEVEL/POLARITY Truth Table. The LEVEL and POLARITY signals are only valid when the output voltage is in regulation.

## SMP402

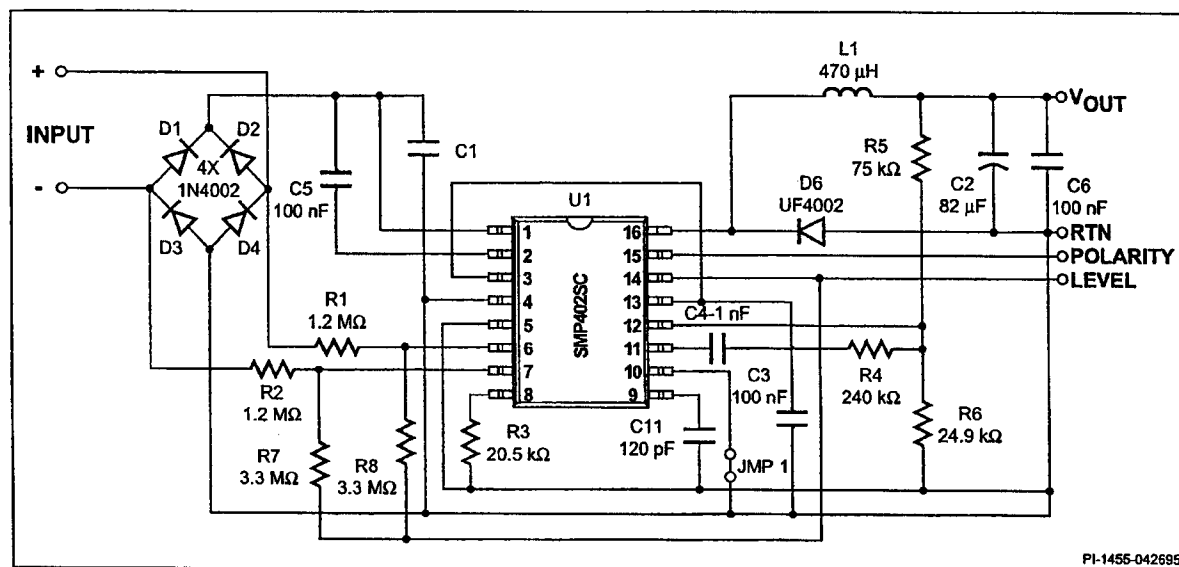


Figure 6. Schematic Diagram of a Non-isolated 5 V, 1 W ISDN Regulator Circuit Utilizing the SMP402.

## General Circuit Operation

The Buck DC-to-DC converter shown in Figure 6 produces a single non-isolated 5 V, 1 W power supply. The high-voltage P-channel MOSFET transistor in the SMP402 is turned on and off at the switching frequency. The ratio of ON-time to the switching period is defined as the duty cycle. The duty cycle changes with input voltage to maintain a constant average value of the switching waveform. The switching waveform is filtered by inductor L1 and capacitor C2 to produce the 5 V output. During the MOSFET ON-time, the switch current and inductor current ramp up at a linear rate. During the P channel MOSFET switch off time, the voltage across L1 reverses, forward biasing D6. Inductor and diode current then ramp down linearly until the MOSFET turns on again. During normal operation, inductor current ramps up and down around the average value ( $I_{OUT}$ ), which is actually the DC load current.

The 5 V output voltage is directly sensed and accurately regulated by an internal error amplifier. The error amplifier generates an error signal which directly controls the duty cycle of the integrated high-voltage P-channel MOSFET switch. The effective output voltage can be fine-tuned by adjusting the resistor divider formed by R5 and R6. Other output voltages are possible (up to approximately half the input voltage) by changing the value of L1 as well as the resistor divider.

Polarity of the DC input voltage can be either positive or negative. D1, D2, D3, and D4 “rectify” the DC input voltage to provide a positive polarity input voltage for the converter. C1 provides input voltage filtering. The SMP402 contains the integrated controller and high-voltage P-channel MOSFET which, together with D6, generates a pulse width modulated switching AC voltage waveform. L1 and C2 filter the AC voltage to create the 5 V output. C6 filters high-frequency noise currents. R5 and R6 sense and divide the 5 V output voltage for comparison with the internal

bandgap reference voltage. C4 and R4 provide control loop compensation feedback around the internal error amplifier. C3 bypasses the onboard  $V_S$  regulator. C11 sets the switching frequency. R3 is fixed to set internal currents accurately. C5 bypasses an internally-generated, level-shifted bias source of approximately 10 V, which is referenced to the positive side of the effective input voltage. This floating supply is used for biasing the P-channel MOSFET gate drivers. R1 and R2 sense the level and polarity of the DC input voltage. The current through R1 and the SENSE+ input or R2 and the SENSE- input must exceed 23  $\mu$ A before the converter will turn on. R7 and R8 provide hysteresis for the SENSE+ and SENSE- inputs. Jumper JMP1 disables the self-bias feature of the SMP402.

## General Circuit Operation (cont.)

The line and load regulation graphs were measured on the circuit shown in Figure 6. The switching frequency of the power supply was measured at 230 kHz.

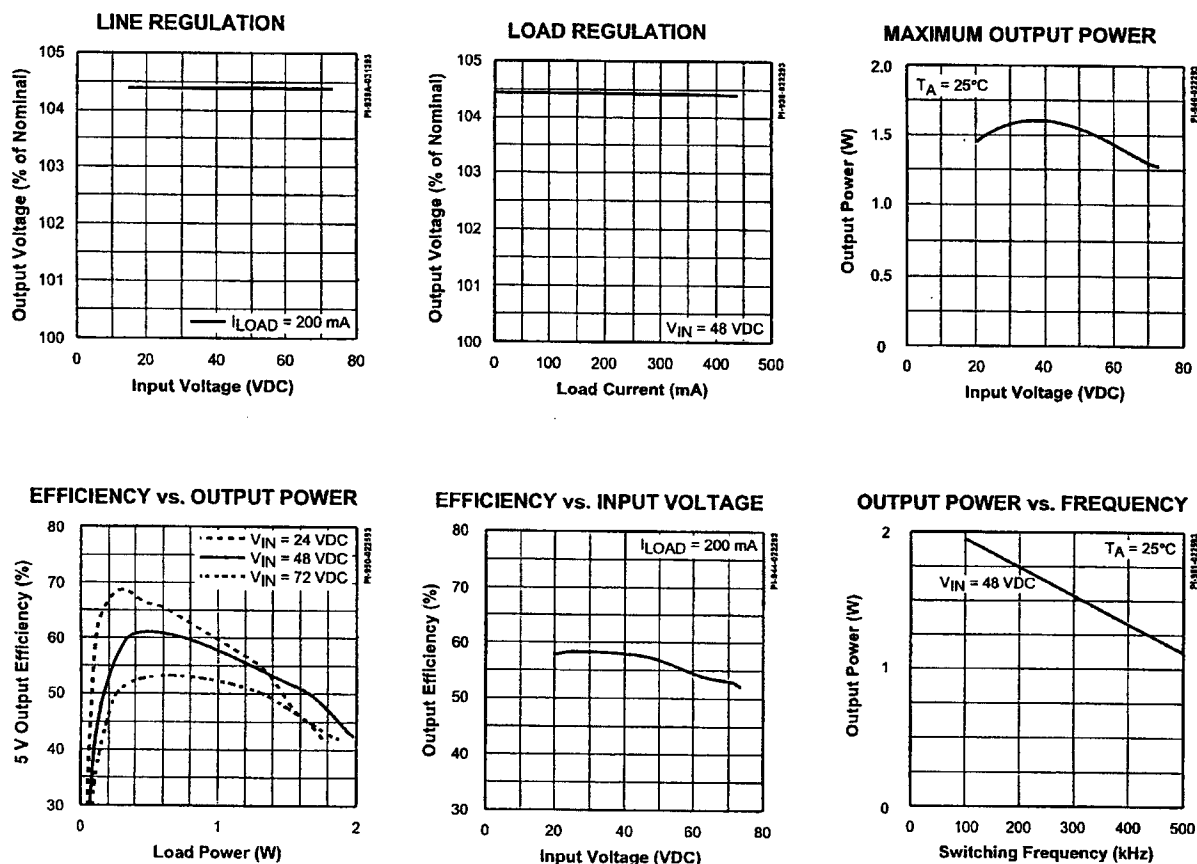
The maximum output power curve shows

the power output capability for a 470  $\mu$ H output filter inductor (L1).

The output power versus frequency curve was generated by characterization of the SMP402 at various frequencies. The

curve demonstrates the trade-off between AC and DC power losses within the device. As AC losses rise with frequency, DC losses and output power must be reduced to maintain the same device maximum power dissipation.

## Typical Performance Characteristics (Figure 6 Power Supply)





**SMP402****ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

$V_{IN}$ Voltage .....	80 V	Lead Temperature <sup>(3)</sup> .....	260°C
Drain-Source Voltage ( $V_{IN}$ to OUT) .....	90 V	Power Dissipation .....	1.0 W
$V_{BIAS}$ Voltage .....	5.5 V	Thermal Impedance ( $\theta_{JA}$ ) .....	55°C/W
SENSE Current .....	$\pm 200 \mu A$	Thermal Impedance ( $\theta_{JC}$ ) <sup>(4)</sup> .....	15°C/W
OUT Voltage .....	$V_{IN} + 0.3 V$ to $-4 V$	1. Unless noted, all voltages referenced to A GND, $T_A = 25^\circ C$ 2. Normally limited by internal circuitry. 3. 1/16" from case for 5 seconds. 4. Measured at pin 4/5.	
OUT Current .....	250 mA		
Logic Input Voltage .....	$-0.3 V$ to $V_S + 0.3 V$		
Storage Temperature .....	$-65$ to $125^\circ C$		
Operating Junction Temperature <sup>(2)</sup> .....	0 to $150^\circ C$		

Parameter	Symbol	Conditions	Min	Typ	Max	Units
		(Unless Otherwise Specified) $V_{IN} = 48\text{ V}$ , $V_{BIAS} = 5\text{ V}$ , $GNDs = 0\text{ V}$ $R_{EXT} = 20.5\text{ k}\Omega$ , $C_{EXT} = 120\text{ pF}$ $R_{S+}$ , $R_{S-} = 1.2\text{ M}\Omega$ , $T_J = 0\text{ to }120^{\circ}\text{C}$				
OSCILLATOR						
Output Frequency	$f_{OSC}$	$C_{EXT} = 30\text{ to }300\text{ pF}$	50		500	kHz
Initial Accuracy	$\Delta f_{OSC}$		200	230	260	kHz
PULSE WIDTH MODULATOR						
Duty Cycle	DC		0-50	0-70		%
ERROR AMPLIFIER						
Threshold Voltage	$V_{REF}$		1.22		1.32	V
Gain-Bandwidth Product				0.5		MHz
DC Gain	$A_{VOL}$		60	80		dB
Common-mode Range	$V_{EA\ IN}$	See Note 2	0		3	V
Output Impedance	$Z_{OUT}$			1		k $\Omega$



**SMP402**

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
		(Unless Otherwise Specified) $V_{IN} = 48\text{ V}$ , $V_{BIAS} = 5\text{ V}$ , $GNDs = 0\text{ V}$ $R_{EXT} = 20.5\text{ k}\Omega$ , $C_{EXT} = 120\text{ pF}$ $R_{S+}, R_{S-} = 1.2\text{ M}\Omega$ , $T_j = 0\text{ to }120^{\circ}\text{C}$					
CIRCUIT PROTECTION							
Thermal Shutdown Temperature		$V_{IH} = 3.0\text{ V}$	120	140		$^{\circ}\text{C}$	
Thermal Shutdown Hysteresis		$V_{IL} = 0\text{ V}$		15		$^{\circ}\text{C}$	
LOGIC							
Input Current High	$I_{IH}$			10	50	$\mu\text{A}$	
Input Current Low	$I_{IL}$		-500	-100		$\mu\text{A}$	
Input Voltage High	$V_{IH}$				3.0	V	
Input Voltage Low	$V_{IL}$		1.0			V	
Output Voltage High	$V_{OH}$	$I_{OH} = -0.5\text{ mA}$	3.5			V	
Output Voltage Low	$V_{OL}$	$I_{OL} = 0.5\text{ mA}$			0.4	V	
SENSE INPUTS							
Threshold Voltage	$V_{SENSE+/-}$			1.7	2.2	V	
LEVEL Threshold Current	$I_{LEVEL}$		21	24	27	$\mu\text{A}$	
POLARITY Threshold Current	$I_{POLARITY}$			5	7	$\mu\text{A}$	
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	$I_{OUT} = -100\text{ mA}$	$T_j = 25^{\circ}\text{C}$			12	$\Omega$
			$T_j = 100^{\circ}\text{C}$			20	
ON-State Current	$I_{D(ON)}$	$V_{DS} = 5\text{ V}$ See Note 1	$T_j = 25^{\circ}\text{C}$	200	500		mA
			$T_j = 100^{\circ}\text{C}$	100	350		



**SMP402**

Parameter	Symbol	Conditions (Unless Otherwise Specified) $V_{IN} = 48\text{ V}$ , $V_{BIAS} = 5\text{ V}$ , $GNDs = 0\text{ V}$ $R_{EXT} = 20.5\text{ k}\Omega$ , $C_{EXT} = 120\text{ pF}$ $R_{S+}$ , $R_{S-} = 1.2\text{ M}\Omega$ , $T_J = 0\text{ to }120^\circ\text{C}$	Min	Typ	Max	Units
<b>OUTPUT (cont.)</b>						
OFF-State Current	$I_{DSS}$	$V_{IN} = 72\text{ V}$ , $OUT = 0\text{ V}$ , $T_A = 120^\circ\text{C}$	-50	-10		$\mu\text{A}$
Breakdown Voltage	$BV_{DSS}$	$I_{OUT} = -250\text{ }\mu\text{A}$ , $T_A = 25^\circ\text{C}$	90			V
<b>SUPPLY</b>						
HV Regulator Voltage	$V_{IN}$		12		72	V
Off-line Supply Current	$I_{IN}$	$V_{BIAS} = \text{A GND}$		1.5	2.5	mA
		$V_{BIAS} = 5\text{ V}$		1	1.5	
$V_{BIAS}$ Supply Voltage	$V_{BIAS}$		4.75		5.25	V
$V_{BIAS}$ Supply Current	$I_{BIAS}$			1	1.5	mA

**NOTES:**

1. At low output currents (< 20 mA), the part may operate in blocking oscillation mode, resulting in large output ripple.
2. Applying >3.5 V to the EA IN pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the SMP402 is connected to a high voltage power source when the test circuit is activated.

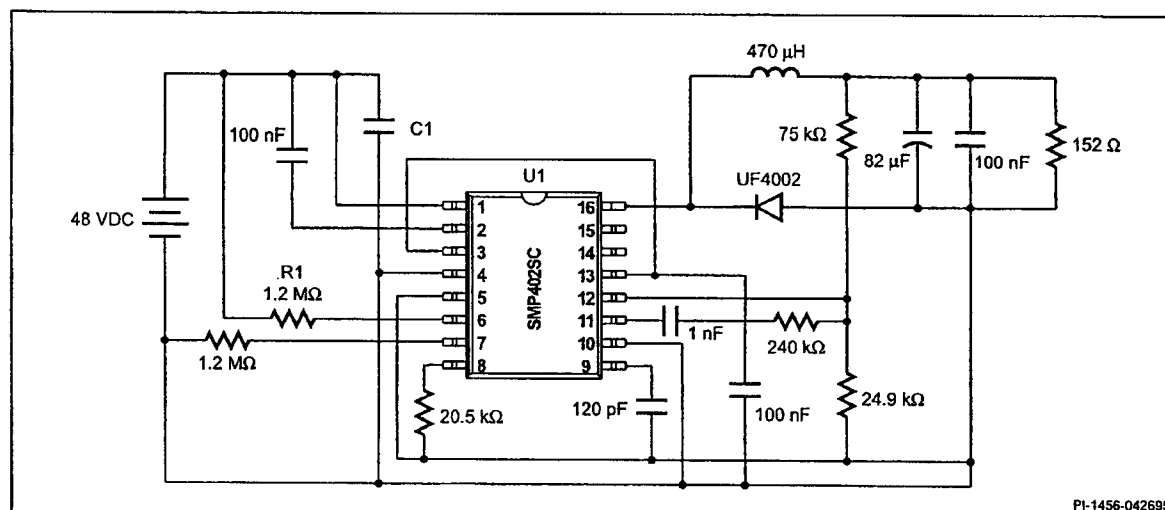
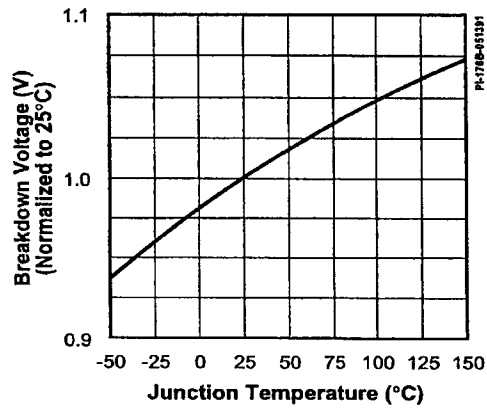
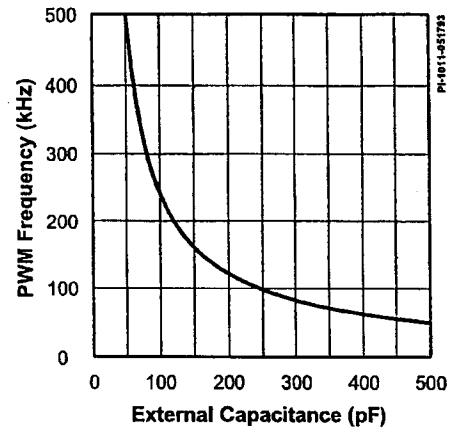
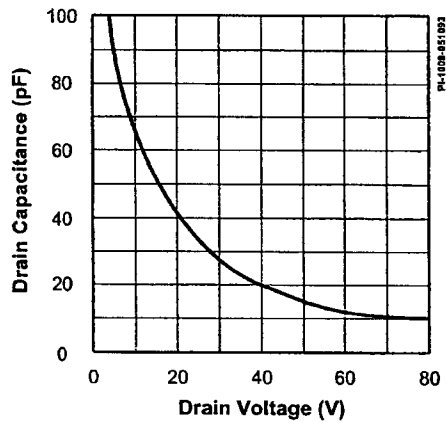
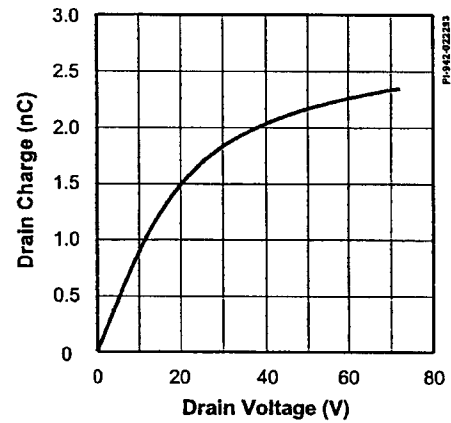
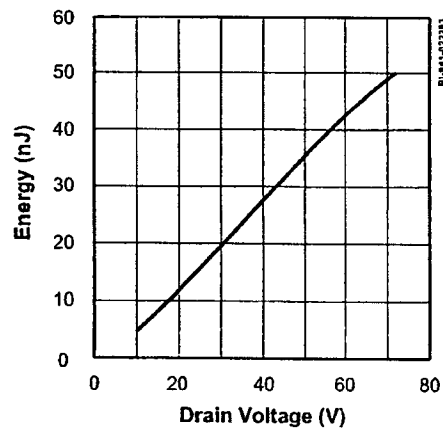
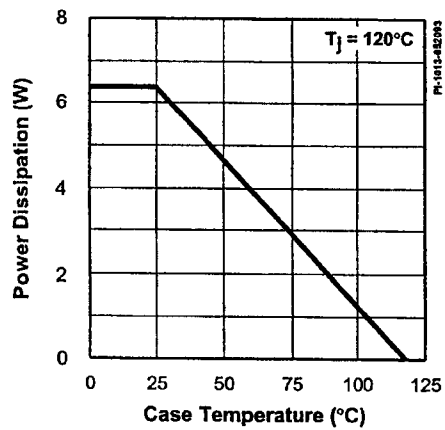
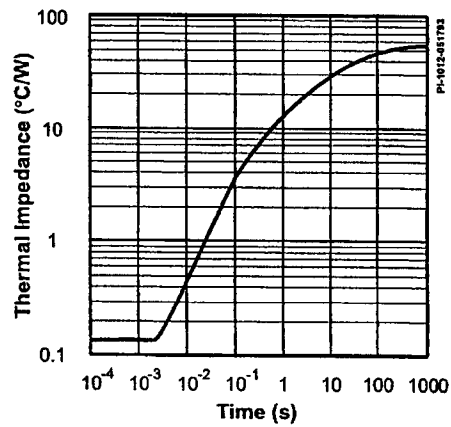


Figure 7. Switching Time Test Circuit.

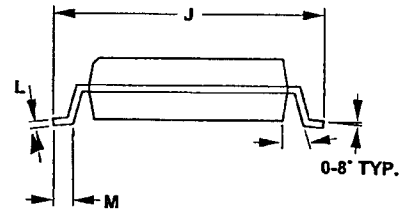
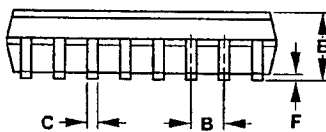
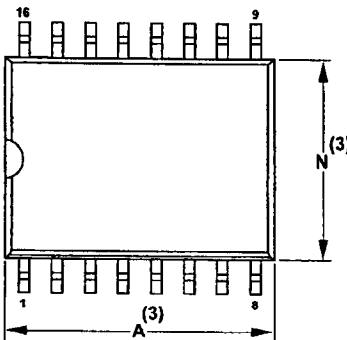
**SMP402****BREAKDOWN vs. TEMPERATURE****f<sub>PWM</sub> vs. EXTERNAL CAPACITANCE****C<sub>oss</sub> vs. DRAIN VOLTAGE****DRAIN CHARGE vs. DRAIN VOLTAGE****DRAIN CAPACITANCE ENERGY**

**SMP402****PACKAGE POWER DERATING****TRANSIENT THERMAL IMPEDANCE****S16A****Plastic SO-16 (W)**

DIM	inches	mm
A	.398-.413	10.10-10.50
B	.050 BSC	1.27 BSC
C	.014-.018	0.36-0.46
E	.093-.104	2.35-2.65
F	.004-.012	0.10-0.30
J	.394-.418	10.01-10.62
L	.009-.012	0.23-0.32
M	.020-.040	0.51-1.02
N	.291-.299	7.40-7.60

**Notes:**

1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50 mm (.300 inch) body width (issue A, June 1985).
2. Controlling dimensions are in mm.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006 inch) on any side.
4. Pin 1 side identified by chamfer on top edge of the package body or indent on Pin 1 end.



PI-1846-050196



SMP402

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## NOTES



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## NOTES



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## NOTES



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FCS0525820



**SMP402**

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